REMARKS/AGRUMENTS

Reconsideration of this application as amended is respectfully requested.

Claims 1-4, and 12-14, 23-26 and 34-37 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,128,318 to Sato ("Sato").

Claims 5-11, 15-21, 27-33, 38-44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

CLAIM REJECTIONS – 35 USC §102 (e)

The Examiner has rejected claims 1-4, and 12-14, 23-26 and 34-37 under 35 U.S.C. §102(e) as being anticipated by Sato. Applicants submit that claims 1-4, and 12-14, 23-26 and 34-37 are not anticipated by Sato. In regard to the rejection of claim 1, 12, 23, 24, the Examiner has stated in part that:

> The claimed components comprising line and/or switch cards is disclosed by interface for asynchronous data transfer between cycle slave node and cycle master node and interfaces within nodes.
> (10/21/03, Office Action, p. 2)

Applicants respectfully disagree and submit that amended claim 1 is not anticipated by Sato. Sato describes a method for synchronizing a cycle master node to a cycle slave node using synchronization information from an external network or subnetwork which is supplied to the cycle slave node. (Sato, title) In his background section, Sato explains the network in which his invention is implemented. Specifically, network components are interconnected by a local bus, such as an IEEE 1394 bus to form a subnetwork. (Sato, col. 1, ll. 15-33) Sato provides a mechanism to synchronize a cycle master node to one of the cycle slave nodes within a 1394 network which includes one or more 1394 sub-networks. (Sato, col. 1, ll. 59-63). Thus, Sato

does not contemplate "line and/or switch cards of a communications switch" as stated by applicants in claim 1.

Additionally, amended claim 1 recites the feature of "*wherein the **local clock generating circuit** can switch between a plurality of states, the plurality of states including the synchronization state, and an **alarm state**.*" (Emphasis added) This feature is not disclosed by Sato, as shown by the following analysis. Sato describes synchronizing a cycle timer value of a cycle master node in a 1394 node with an external synchronous cycle reset signal from a 1394 bridge portal. (Sato, col. 5, ll. 54-57). More specifically, Sato provides a control algorithm that corrects for overflow and underflow conditions, and adjusts the cycle timer accordingly. (Sato, col. 5, ll. 32-46) Nowhere in his patent does Sato contemplate "a plurality of states including the synchronization state and an alarm state" as claimed by applicants. Therefore, Sato does not disclose "*wherein the **local clock generating circuit** can switch between a plurality of states, the plurality of states including the synchronization state, and an **alarm state**, and wherein the components comprise line and/or switch cards of **a communications switch**.*" as taught by claim 1. Because Sato does not disclose these features as taught by claim 1, applicants respectfully submit that claim 1 and claims 2-11 which depend from claim 1, are not anticipated under 35 U.S.C. §102(e) by Sato.

The Examiner also rejected independent claim 12 under 35 U.S.C. §102(e) for the reasons set forth in the rejection of claim 1. Amended claim 12 discloses substantially similar limitations as claim 1, and recites "*wherein the **local clock generating circuit** can switch between a plurality of states, the plurality of states including the synchronization state, and an **alarm state**, and wherein the components comprise line and/or switch cards of **a communications switch**.*" (Emphasis added) Because Sato does not disclose this feature as taught by applicants' claim 12 from which claims 13-21 depend, for the reasons discussed above with regard to claim

1, applicants respectfully submit that claims 12-21 are not anticipated under 35 U.S.C. §102(e) by Sato.

The Examiner also rejected independent claim 23 under 35 U.S.C. §102(e) for the reasons set forth in the rejection of claim 1. Amended claim 23 discloses substantially similar limitations as claim 1, and recites "*wherein the **local clock generating circuit** can switch between a plurality of states, the plurality of states including the synchronization state, and an **alarm state**, and wherein the components comprise line and/or switch cards of **a communications switch**.*" (Emphasis added) Because Sato does not disclose this feature as taught by applicants' claim 23 from which claims 24-33 depend, for the reasons discussed above with regard to claim 1, applicants respectfully submit that claims 23-33 are not anticipated under 35 U.S.C. §102(e) by Sato.

The Examiner also rejected independent claim 34 under 35 U.S.C. §102(e) for the reasons set forth in the rejection of claim 1. Amended claim 34 discloses substantially similar limitations as claim 1, and recites "*wherein the **local clock generating circuit** can switch between a plurality of states, the plurality of states including the synchronization state, and an **alarm state**, and wherein the components comprise line and/or switch cards of **a communications switch**.*" (Emphasis added) Because Sato does not disclose this feature as taught by applicants' claim 34 from which claims 35-44 depend, for the reasons discussed above with regard to claim 1, applicants respectfully submit that claims 34-44 are not anticipated under 35 U.S.C. §102(e) by Sato.

For the foregoing reasons, applicant respectfully submits that the applicable objections and rejections have been overcome and that the claims are in condition for allowance. If there are any additional charges, please charge them to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: February 23, 2004 Sanjeet Dutta

Sanjeet K. Dutta
Reg. No. 46,145

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025
(408) 947-8200